High-Speed 10-bit PXI/CompactPCI Digitizers

- **DC282**
  - 10-bit
  - 4 ch
  - 8 GS/s

- **DC252**
  - 10-bit
  - 2 ch
  - 8 GS/s

- **DC222**
  - 10-bit
  - 1 ch
  - 8 GS/s

ASBus²
Ctrl I/O

XLFidelity JetSpeed II Technology
The DC282, DC252 and DC222 PXI/CompactPCI 10-bit digitizers can each achieve a dazzling single-channel sampling rate of 8 GS/s, and offer a choice of front-end input mezzanines providing up to 3 GHz input bandwidth or switchable high impedance input coupling. This front-end flexibility, coupled with astounding data conversion performance, makes these digitizers ideal for implementation in applications such as high-resolution radar, lidar, and ultrasound, as well as semiconductor test and large scale physics research experiments.

The DC282 offers synchronous four channel sampling at up to 2 GS/s, or interleaved dual- or single-channel sampling at up to 4 and 8 GS/s respectively. The DC252 and DC222 digitizers offer the same dual- and single-channel sampling performance, with the model DC222 achieving 8 GS/s on its single input channel. These digitizers are fully compliant with both the PXI and CompactPCI standards, and incorporate Acqiris’ proprietary XLFidelity and JetSpeed II ADC chipsets, designed for the specific purpose of optimizing high-speed ADC performance.

The three modules combine this ultra fast sampling rate with standard acquisition memories of 256 kpoints (DC282), 512 kpoints (DC252), to 1 Mpoints (DC222) per channel, and optional acquisition memories to 256 Mpoints, 512 Mpoints and 1 Gpoints, respectively.

Main Features

- Quad-, dual- and single-channel models
- Up to 8 GS/s sampling rate with 10-bit ADC resolution
- Choice of mezzanine front ends with input protection
- Standard input option, 2 GHz bandwidth, 50 Ω, DC or AC-coupled, with internal DC calibration
- High-frequency input option, 3 GHz bandwidth, 50 Ω, DC-coupled
- High-impedance input option, 1 GHz bandwidth, 50 Ω / 1 MΩ, DC or AC-coupled with internal DC calibration
- Acquisition memory from 256 kpoints to 1 Gpoints (optional)
- 2 GHz Auto-Synchronous Bus system (ASBus²) for trigger and clock signal distribution to multiple modules
- Multipurpose I/O connectors for trigger, clock, reference and control signals
- Low dead time (350 ns) sequential recording with time stamps
- Built-in high-resolution Trigger Time Interpolator (TTI) for accurate timing measurements
- Modular, 6U PXI/CompactPCI Standard
- High-speed 64-bit PCI bus transfers data at sustained rates up to 400 MB/s to host PC
- Device drivers for Windows 2000/XP, LabView RT, Wind River VxWorks, and Linux (support for other operating systems on request)
- Drivers with application code examples for LabWindows/CVI, LabVIEW, C/C++ and Microsoft Visual Basic
- Software adapter for MATLAB

High-Resolution High Sample Rate Signal Acquisition

The DC282, DC252 and DC222 PXI/CompactPCI 10-bit digitizers can each achieve a dazzling single-channel sampling rate of 8 GS/s, and offer a choice of front-end input mezzanines providing up to 3 GHz input bandwidth or switchable high impedance input coupling. This front-end flexibility, coupled with astounding data conversion performance, makes these digitizers ideal for implementation in applications such as high-resolution radar, lidar, and ultrasound, as well as semiconductor test and large scale physics research experiments.
Multiple Front-End Options

As with other Acqiris products, the entire front end is mounted on a removable mezzanine card so, in the event of accidental damage or as relays fatigue over time, replacement is fast and efficient. The DC282, DC252 and DC222 offer a choice of standard, high-frequency and high-impedance front-end mezzanines, each with a choice of BNC or SMA connectors.

The 50 Ω digitizing channel of the Standard front end is fully protected against overvoltage signals. Programmable front-end electronics are used to provide a complete set of input voltage ranges, from 50 mV to 5 V full scale (in a 1, 2, 5 sequence) with variable voltage offset. With bandwidth of 2 GHz, amplifier response (flatness, overshoot and accuracy) are optimized to ensure that high-frequency measurements can be made with the greatest precision and confidence. The front-end circuitry features internal calibration (no need to disconnect input signals), switchable filtering and very fast recovery from out-of-range signals.

The DC282, DC252 and DC222 offer a choice of standard, high-frequency and high-impedance front-end mezzanines, each with a choice of BNC or SMA connectors.

A direct access to the **XLFidelity** cross point switch, is provided via the High-frequency input front end. In order to benefit from the full bandwidth of the CPS and Atmel AT84AS008GL ADC there is minimal signal conditioning, the full scale range fixed at 1 V. The input channel has an overvoltage protection to ±2 V.

High voltage measurements are possible with the High-impedance front-end option. Programmable front-end electronics are used to provide a complete set of input voltage ranges, from 50 mV to 5 V full scale into 50 Ω, and up to 50 V full scale into 1 MΩ impedance. With a bandwidth of 1 GHz (typ.) into 50 Ω, and 300 MHz into 1 MΩ, the amplifier response is optimized and the front-end circuitry allows the same internal calibration as the Standard 50 Ω front-end mezzanine, with switchable filtering and very fast recovery from out-of-range signals.

### Multiple Front-End Options

<table>
<thead>
<tr>
<th>Front-End Mezzanine Selection</th>
<th>Input Impedance</th>
<th>Bandwidth</th>
<th>Full Scale Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-Frequency (-HF)</td>
<td>50 Ω</td>
<td>3 GHz</td>
<td>1 V</td>
</tr>
<tr>
<td>Standard (-Std)</td>
<td>50 Ω</td>
<td>2 GHz</td>
<td>50 mV, 100 mV, 200 mV, 500mV, 1 V, 2 V, and 5 V</td>
</tr>
<tr>
<td>High-Impedance (-HZ)</td>
<td>50 Ω/1MΩ</td>
<td>1 GHz/300 MHz</td>
<td>50 Ω and 1 MΩ: 50 mV, 100 mV, 200 mV, 500 mV, 1 V, 2 V, 5 V 1 MΩ only: 10 V, 20 V, 50 V</td>
</tr>
</tbody>
</table>

**Integrated Acqiris Technology**

**Dedicated ADC Chipsets**

Acqiris ADC chipsets are designed for the specific purpose of optimizing high-speed ADC performance. The **XLFidelity** ADC front-end chipset integrates the signal conditioning, amplification, and interleaving functions essential to high-speed data acquisition into two companion ASIC devices, allowing the accurate interleaving of up to 4 high-speed ADCs.

**JetSpeed II** represents the next generation in Acqiris’ dedicated ADC chipsets. It is designed to enhance high-speed ADC performance through the distribution of accurate synchronization and time base signals along with memory acquisition and control functions to increase the data throughput from the acquisition to internal memory.
**Extended Functionality**

**Multi GHz Bandwidth Front End**
Both the standard and high-impedance front-end mezzanines include the XL*Fidelity* front-end amplifier chip. This circuit includes a programmable gain amplifier (PGA) with on-chip filtering and trigger circuitry. It provides pre-ADC signal conditioning and amplification, essential for high performance high-speed data conversion systems.

The PGA provides five global gain settings: 1.0, 2.0, 2.5, 5.0, and 10.0. The filter section, which is useful for signal noise reduction, allows 2-pole Bessel bandwidth limiting at 700 MHz and 200 MHz and a single-pole filter at 20 MHz.

**Trigger Mezzanine with I/O Ports**
The trigger mezzanine includes the XL*Fidelity* front-end amplifier chip. The trigger processing circuit embedded in the package includes dual comparators for window triggering mode, on chip DACs for threshold adjustment, additional filters for LF and HF reject trigger coupling, and a prescaler to allow a HF divide by 4 mode.

The trigger mezzanine provides access to the circuit via a standard 50 Ω terminated BNC or SMA connector and Ctrl I/O. These four front-panel MMCX connectors provide access for an external clock or 10 MHz reference signal, a trigger output and two additional I/O digital control lines (I/O A & B) for monitoring or modifying the digitizer’s status and configuration or to extract a 10 MHz clock signal.

**Auto-Synchronous Bus System**
If more than four synchronous data acquisition channels are required, digitizers can be combined using Acqiris’ ASBus².

This proprietary high-bandwidth auto-synchronous bus system provides direct access to the digitizer’s on-board JetSpeed II clock distribution circuit. ASBus² connects multiple digitizer clock circuits and synchronizes the on-board PLLs to a common master clock.
Precise Channel Interleaving

The XL\textit{Fidelity} cross point switch chip, can be simply described as a matrix of analog multiplexers. It includes a calibration input, essential for the accurate timing calibration of several interleaved ADCs, and allows offset matching with four dedicated on-chip 8-bit DACs.

The interleaving of multiple ADCs is essential for high-speed data conversion systems. The process increases the effective sample rate available in high-speed digitizer systems by acquiring the same signal on two or more high-speed ADCs, in parallel and out of phase. These acquired signals must then be reordered and recombined to reconstruct the signal waveform.

Fast Data Throughput

The Jet\textit{Speed II} Memory and Acquisition Controller, is a digital CMOS integrated circuit. A high-speed data demultiplexer with on-board memory, it is designed for the capture and memorization of 10-bit digital data, at speeds of up to 2 GS/s. It has large internal static RAMs, high clock frequencies, and is able to accept and generate LVDS (low-voltage differential signal, 100 mV - 600 mV range) levels for fast input/output signals.

The circuit allows storage of the input data stream to a self-addressed 10-bit 256 kpoints internal memory. The DC282, DC252 and DC222 digitizers have provisions for an external memory expansion of up to 1 Gpoints.

Reference Clock and Synchronization

The Jet\textit{Speed II} clock distribution circuit includes trigger functions to facilitate high performance triggering on specific signal waveforms. The chip is designed for use with the Jet\textit{Speed II} Memory and Acquisition Controller chip, to interleave up to 4 high-speed ADCs to achieve unmatched high-speed data acquisition performance.
# High-Speed 10-bit PXI/CompactPCI Digitizer

## Model DC282
Quad-channel, 10-bit, 2-8 GS/s, 256-1024 kpoint, 32-128 Mpoint or 256-1024 Mpoint memory

## Model DC252
Dual-channel, 10-bit, 4-8 GS/s, 512-1024 kpoint or 512-1024 Mpoint memory

## Model DC222
Single-channel, 10-bit, 8 GS/s, 1024 kpoint or 1024 Mpoint memory

### Standard Input: 50 Ω (-Std Front-End Option)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth (-3 dB)</td>
<td>DC to 2 GHz</td>
</tr>
<tr>
<td>Full Scale (FS)</td>
<td>50 mV to 5 V</td>
</tr>
<tr>
<td>Offset Range</td>
<td>±2 V to ±5 V</td>
</tr>
<tr>
<td>Bandwidth Limit Filters</td>
<td>700 MHz, 200 MHz and 20 MHz</td>
</tr>
<tr>
<td>Maximum Input Voltage</td>
<td>±5 V DC</td>
</tr>
<tr>
<td>Impedance</td>
<td>50 Ω ±1% @ DC</td>
</tr>
<tr>
<td>Coupling</td>
<td>DC, AC (32 Hz LF limit, 50 Ω)</td>
</tr>
<tr>
<td>SFDR (typ.)</td>
<td>&gt; 52 dB @ 10 MHz</td>
</tr>
<tr>
<td>SNR (typ.)</td>
<td>40 dB full bandwidth</td>
</tr>
<tr>
<td>DC Accuracy</td>
<td>± (2% x FS + 0.4% x offset)</td>
</tr>
<tr>
<td>Effective Bits (typ. @ 2 GS/s)</td>
<td>7.2: DC - 10 MHz, 20 MHz BWL, 6.9: 10 - 100 MHz, 200 MHz BWL, 6.5: 100 - 400 MHz, full bandwidth, 5.4: 0.4 - 1 GHz, full bandwidth</td>
</tr>
</tbody>
</table>

### High-Frequency Input: 50 Ω (-HF Front-End Option)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth (-3 dB)</td>
<td>DC to 3 GHz</td>
</tr>
<tr>
<td>Full Scale (FS)</td>
<td>1 V</td>
</tr>
<tr>
<td>Offset Range</td>
<td>±0.5 V</td>
</tr>
<tr>
<td>Maximum Input Voltage</td>
<td>±2 V DC</td>
</tr>
<tr>
<td>Impedance</td>
<td>50 Ω ±2% @ DC</td>
</tr>
<tr>
<td>Coupling</td>
<td>DC</td>
</tr>
<tr>
<td>SFDR (typ.)</td>
<td>&gt; 57 dB @ 10 MHz</td>
</tr>
<tr>
<td>SNR (typ.)</td>
<td>47 dB full bandwidth</td>
</tr>
<tr>
<td>DC Accuracy</td>
<td>± (2% x FS + 1% x offset)</td>
</tr>
<tr>
<td>Effective Bits (typ. @ 2 GS/s)</td>
<td>6.8: DC - 400 MHz, full bandwidth, 6.1: 0.4 - 1 GHz, full bandwidth, 5.7: 1 - 2 GHz, full bandwidth</td>
</tr>
</tbody>
</table>

### High-Impedance Input: 50 Ω/1 MΩ (-HZ Front-End Option)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth (-3 dB)</td>
<td>50 Ω: DC to 1 GHz (typ.), 1 MΩ: DC to 300 MHz (typ.)</td>
</tr>
<tr>
<td>Full Scale (FS)</td>
<td>50 Ω: 50 mV to 5 V, 1 MΩ: 50 mV to 50 V</td>
</tr>
<tr>
<td>Offset Range</td>
<td>±5 Ω: ±2 V to ±5 V, 1 ΜΩ: ±2 V to ±200 V</td>
</tr>
<tr>
<td>Bandwidth Limit Filters</td>
<td>50 Ω: 700 MHz, 200 MHz and 20 MHz, 1 MΩ: 20 MHz</td>
</tr>
<tr>
<td>Maximum Input Voltage</td>
<td>±5 V DC</td>
</tr>
<tr>
<td>Impedance</td>
<td>50 Ω ± 1.0 % @ DC, 1 MΩ ± 1.0 % @ DC</td>
</tr>
<tr>
<td>Coupling</td>
<td>DC, AC</td>
</tr>
<tr>
<td>SFDR (typ. @ 2 GS/s, 50 Ω)</td>
<td>&gt; 59 dB @ 10 MHz</td>
</tr>
<tr>
<td>SNR (typ. 50 Ω)</td>
<td>36 dB full bandwidth</td>
</tr>
<tr>
<td>DC Accuracy</td>
<td>± (2% x FS + 0.4% x offset)</td>
</tr>
<tr>
<td>Effective Bits (typ. @ 2 GS/s, 50 Ω)</td>
<td>6.9: DC - 10 MHz, 20 MHz BWL, 6.6: 10 - 100 MHz, 200 MHz BWL, 6.2: 100 - 400 MHz, full bandwidth</td>
</tr>
</tbody>
</table>

### Digital Conversion

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample Rate</td>
<td>100 S/s to 2 GS/s in 1, 2, 2.5, 5 sequence and 4 GS/s, 8 GS/s</td>
</tr>
<tr>
<td>Resolution</td>
<td>10 bits (1:1024)</td>
</tr>
<tr>
<td>Integral Nonlinearity (typ.)</td>
<td>±1 LSB</td>
</tr>
<tr>
<td>Acquisition Memory</td>
<td>DC282: 256 kpoints/channel, DC252: 512 kpoints/channel, DC222: 1024 kpoints</td>
</tr>
<tr>
<td>Maximum Optional Memory</td>
<td>DC282: 256 Mpoints/channel, DC252: 512 Mpoints/channel, DC222: 1024 Mpoints</td>
</tr>
</tbody>
</table>
### Time Base

**Clock Accuracy**
Better than ±2 ppm

**Sampling Jitter**
< 1 ps RMS
(for 10 µs record length)

**Acquisition Modes**
Single shot, Start-on-trigger, Sequence
(1 to 1200 segments, dead time 350 ns.
125,000 segments with max memory option, dead time: < 1.1 µs with any memory option)

### Internal and External Trigger

**Internal Trigger Input (-Std, -Hz)**
Bandwidth: idem front-end BW
Threshold adjust range: FS of channel
Sensitivity: DC to trigger BW > 15% FS

**Pretrigger**
Adjustable to 100% of horizontal full scale

**Coupling**
DC, AC LF reject (50 Hz),
HF reject (50 kHz)

**External Trigger Input**
Impedance: 50 Ω ±1%
Bandwidth: DC to 2 GHz (-3 dB)
Full Scale: 0.5, 1, 2, 5 V
Threshold Adjust Range: ±FS/2
Maximum input voltage: ±5 V DC
Sensitivity: DC to 2 GHz >15% FS

**Modes**
Edge, positive and negative
HF: divide by 4
Spike stretcher
Window In/Out

**Post-Trigger**
Adjustable up to 2^{35.1} points

A high-speed front-panel bus (ASBus²) distributes clock and trigger to synchronize multiple modules.

### Control I/O

**I/O A & B Signals**
TTL & CMOS compatible (3.3 V)

**I/O A & B Input**
Trigger enable

**I/O A & B Output**
10 MHz reference clock
Acquisition skipping to next segment
Acquisition active
Trigger ready

**CLK IN Input**
200 MHz to 2 GHz
> 500 mV pk-pk into 50 Ω
±5 DC max voltage

**CLK IN Ext. Clock/Ref Threshold**
Variable between -3 V and +3 V

**CLK IN Ext. Reference Frequency**
10 MHz ±0.3 %

**TRG OUT Output Level**
Adjustable in range ±2.5 V (no load)
Amplitude ±0.8 V (no load)
±15 mA max

**TRG OUT Rise/Fall Time**
2.5 ns into 50 Ω

### General

**Operating System**
Windows, VxWorks, LabView RT or Linux

**Transfer Speed**
High-speed PCI bus transfers data at sustained rates up to 400 Mbytes/sec to host PC

**Power Consumption (typ.)**
< 50 W without memory option
< 60 W with memory option

**Warranty**
3 years

**Current Requirements (max.)**

<table>
<thead>
<tr>
<th></th>
<th>Std (W)</th>
<th>HF (W)</th>
<th>HZ (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>±12 V</td>
<td>100 mA</td>
<td>100 mA</td>
<td>100 mA</td>
</tr>
<tr>
<td>±5 V</td>
<td>6.3 A</td>
<td>5.2 A</td>
<td>6.5 A</td>
</tr>
<tr>
<td>±3.3 V</td>
<td>4.2 A</td>
<td>4.2 A</td>
<td>4.2 A</td>
</tr>
<tr>
<td>-12 V</td>
<td>50 mA</td>
<td>50 mA</td>
<td>50 mA</td>
</tr>
</tbody>
</table>

1) DCx2 all ADCs sampling at 2 GS/s, without memory option.

Front-Panel LEDs indicate digitizer status - Green: ready for trigger Yellow: module identification Red: trigger

### Environmental and Physical

**Operating Temperature**
0° to 40°C

**Required Airflow**
> 2 m/s in situ

**Relative Humidity**
5 to 95% (non-condensing)

**Shock**
30 G, half-sine pulse

**Vibration**
5 – 500 Hz, random

**Safety**
Complies with EN61010-1

**EMC Immunity**
Complies with EN61326-1

**EMC Emissions**
Complies with EN61326-1 Class A

**Dimensions**
6U PXI/CompactPCI® standard
233 mm x 160 mm x 20 mm

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² As defined by MIL-PRF-28800F Class 3.

Front panel complies with IEEE1101.10

C.E. Certification and Compliance
## Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC282</td>
<td>Base module for quad-channel, 2-8 GS/s, 256-1024 kpoints</td>
</tr>
<tr>
<td>DC282-Std</td>
<td>Standard front-end for DC282, 2 GHz</td>
</tr>
<tr>
<td>DC282-HZ</td>
<td>High-impedance front-end for DC282, (50 Ω/1 MΩ)</td>
</tr>
<tr>
<td>DC282-M32M</td>
<td>32-128 Mpoint acquisition memory option</td>
</tr>
<tr>
<td>DC282-M256M</td>
<td>256-1024 Mpoint acquisition memory option</td>
</tr>
<tr>
<td>DC282-W5</td>
<td>5-year extended warranty</td>
</tr>
<tr>
<td>DC282-CAL</td>
<td>Calibration certificate</td>
</tr>
<tr>
<td>DC252</td>
<td>Base module for dual-channel, 4-8 GS/s, 512-1024 kpoints</td>
</tr>
<tr>
<td>DC252-Std</td>
<td>Standard front-end for DC252, 2 GHz</td>
</tr>
<tr>
<td>DC252-HF</td>
<td>High-frequency front-end for DC252, 3 GHz</td>
</tr>
<tr>
<td>DC252-M512M</td>
<td>512-1024 Mpoint acquisition memory option</td>
</tr>
<tr>
<td>DC252-M32M</td>
<td>32-128 Mpoint acquisition memory option</td>
</tr>
<tr>
<td>DC252-W5</td>
<td>5-year extended warranty</td>
</tr>
<tr>
<td>DC252-CAL</td>
<td>Calibration certificate</td>
</tr>
<tr>
<td>DC222</td>
<td>Base module for single-channel, 8 GS/s, 1024 kpoints</td>
</tr>
<tr>
<td>DC222-Std</td>
<td>Standard front-end for DC222, 2 GHz</td>
</tr>
<tr>
<td>DC222-HF</td>
<td>High-frequency front-end for DC222, 3 GHz</td>
</tr>
<tr>
<td>DC222-M1G</td>
<td>1024 Mpoint acquisition memory option</td>
</tr>
<tr>
<td>DC222-W5</td>
<td>5-year extended warranty</td>
</tr>
<tr>
<td>DC222-CAL</td>
<td>Calibration certificate</td>
</tr>
</tbody>
</table>

**Accessories**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>XA200</td>
<td>MMGX to BNC cable (1 m)</td>
</tr>
</tbody>
</table>

A front-end option must be selected for each base module at time of order. Items not listed in the current price list may only be available upon specific request. Please contact your local representative for more information.

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For other sales and service representatives around the world, see our website at:  
www.acqiris.com

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