PEN Experiment Trigger System (Years 2010)

Anthony Palladino¹, Martin Lehman¹

¹University of Virginia July 27, 2010

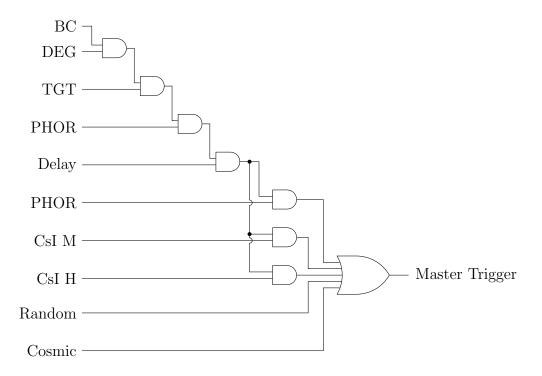


Figure 1: Trigger level 1.

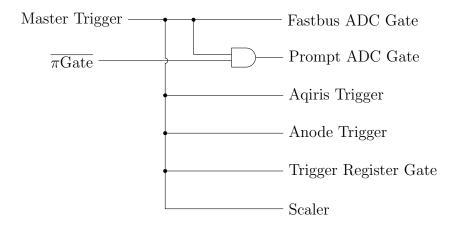


Figure 2: Trigger level 2.

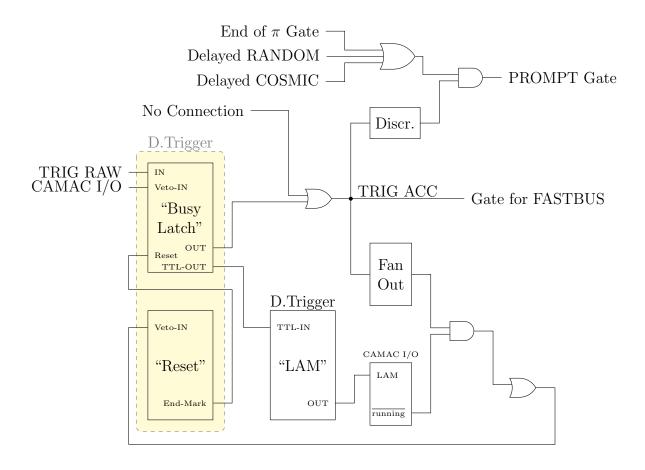


Figure 3: Busy-Latch / Reset Logic.

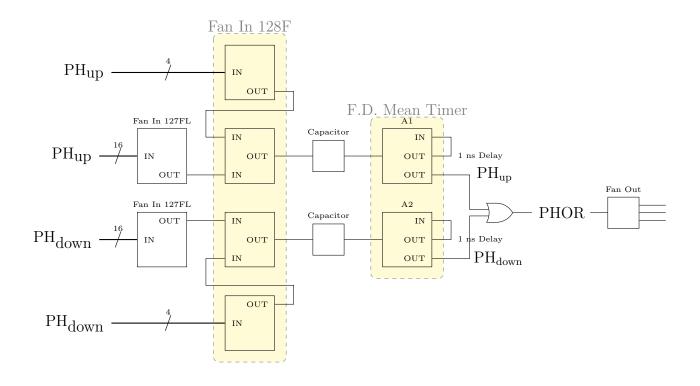


Figure 4: PH Summing.

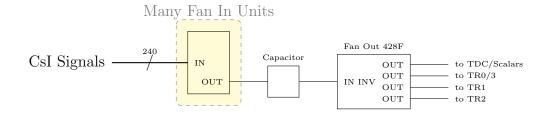


Figure 5: CsI Summing.

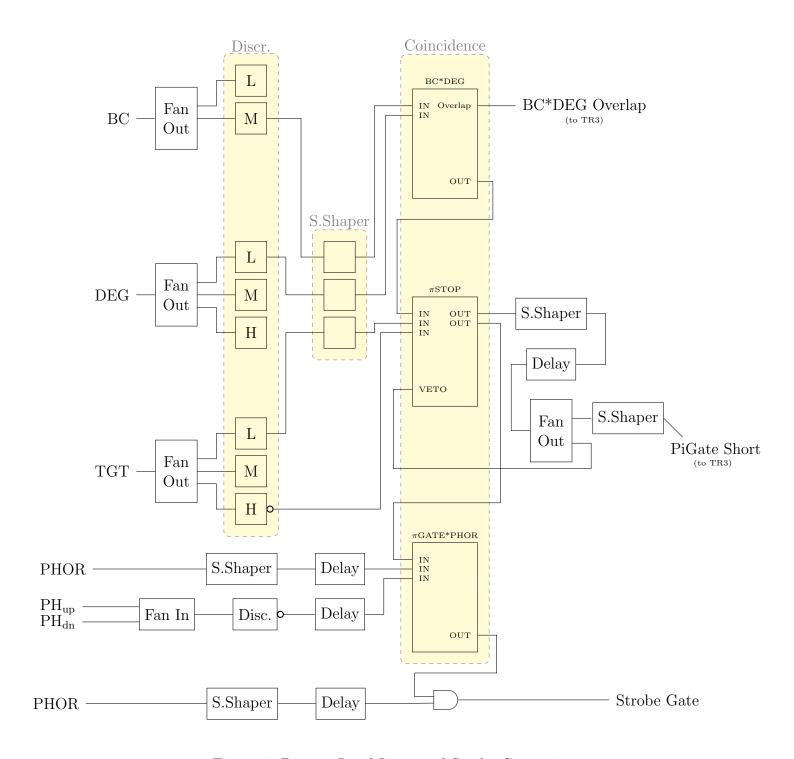


Figure 6: Bottom Level Logic and Strobe Generation.

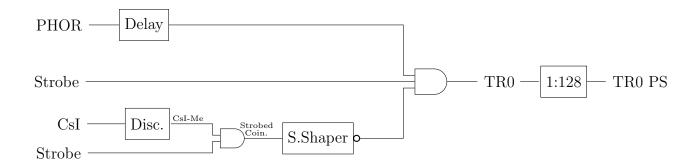


Figure 7: Exclusive TR0.

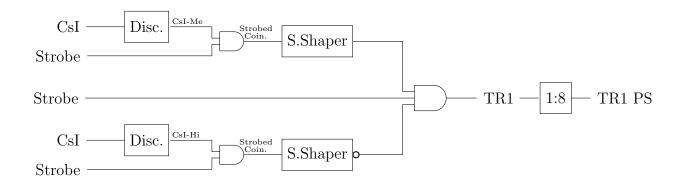


Figure 8: Exclusive TR1.



Figure 9: Exclusive TR2.

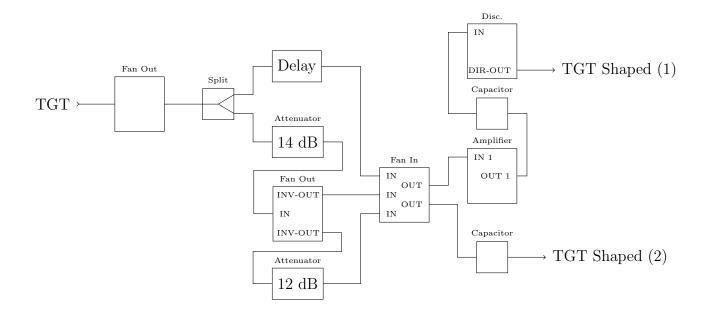


Figure 10: TR3 (part 1) - Target Clip Signal.

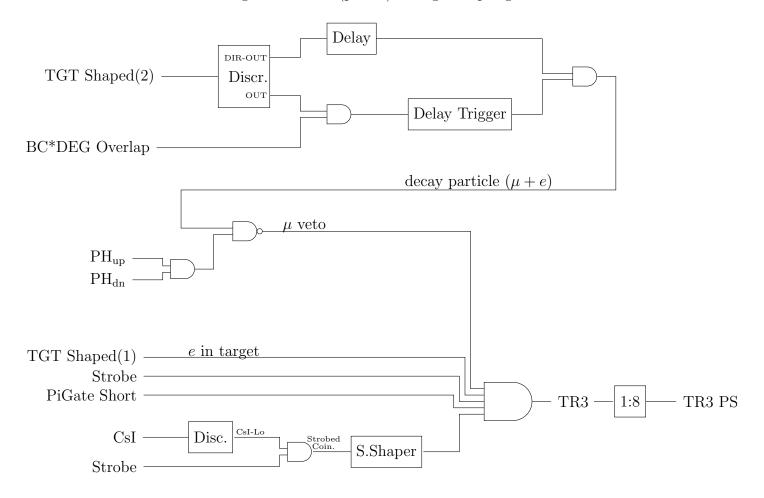


Figure 11: TR3 (part2) - Muon Veto with TR3 Triggers.

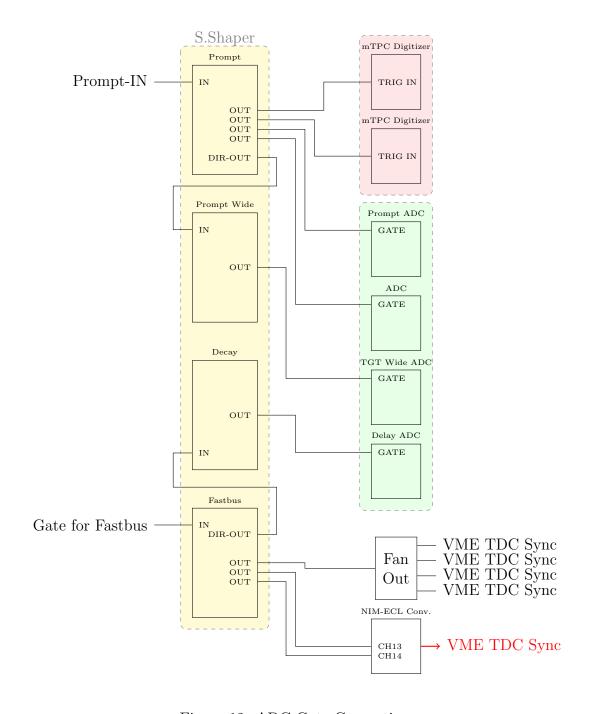


Figure 12: ADC Gate Generation.

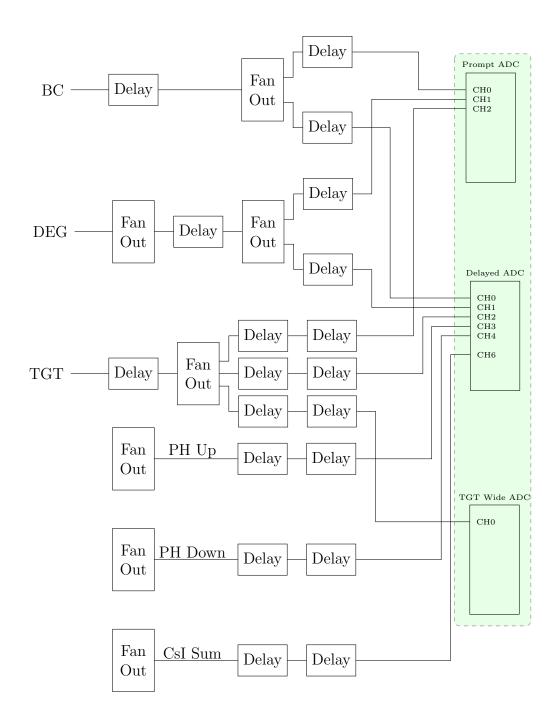


Figure 13: BADC Logic.